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JCS U.S. PTO

June 21, 2000

DOCKET NO.: OGA-172-USAP

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Kazunori ABE et al.

Serial No. TO BE ASSIGNED

Art Unit: TO BE ASSIGNED

Filed: June 21, 2000

Examiner: TO BE ASSIGNED

For: ELECTRONIC ENDOSCOPE SYSTEM ALLOWING ACCURATE DELAY TO BE SET

FORMAL FILING OF NEW PATENT APPLICATION
IN ACCORDANCE WITH 37 CFR §1.53 (b)

Assistant Commissioner of
Patent and Trademarks
Washington, D.C. 20231
BOX: PATENT APPLICATIONS

JCS U.S. PTO
09/599022
06/21/00

Sir:

This application is a:

☒ New Application.

☐ Continuation

☐ Divisional of U.S.P.T.O. Serial Number _____, filed

_____.

☐ Continuation in Part of U.S.P.T.O. Serial Number _____ ,
filed _____.

The undersigned has been authorized by the Applicant(s),

Kazunori ABE

Mitsuru HIGUCHI

FOR: ELECTRONIC ENDOSCOPE SYSTEM ALLOWING ACCURATE DELAY TO BE SET
to file the attached specification and required drawings. Please assign a
serial number and accord a filing date to this prospective application.

June 21, 2000

DOCKET NO.: OGA-172-USAP

Enclosed are:

- 10 pages of Specification,
2 page(s) of Claims,
1 page of an Abstract, and
4 sheet(s) of Drawing(s). Total pages in the disclosure are therefore 17
☒ Return Receipt Postcard.
☒ A combined Declaration and Power of Attorney.
☐ Signed Statement deleting inventor(s) named in prior application.
☐ A verified statement of Status as a Small Entity.
☒ Assignment of the Invention.
☐ This invention is assigned to: (FOR CONTINUATION OR
DIVISIONAL APPLICATION ONLY)
☒ A certified copy of Prior Foreign Application(s).
☐ A Preliminary Amendment.
☐ Letter to the Official Draftsperson and amended drawing(s).
☒ An Information Disclosure Statement and PTO Form 1449.
☒ The basic filing fee of \$690.00.
☐ The fees for the claims to be calculated as follows:

Claims Presented		Less Entitlement		Additional Fees			
				Small Entity		Large Entity	
Total	4	Minus	20	x \$9=	0.00	x \$18=	0.00
Indep.	1	Minus	3	x \$39=	0.00	x \$78=	0.00
New Multiple Dependent Claims		-0-		x\$130=	0.00	x\$260=	0.00
And Claims Dependent Thereon		-0-		x\$130=	0.00	x\$260=	0.00
TOTAL ADDITIONAL FEE				0.00		0.00	

June 21, 2000

DOCKET NO.: OGA-172-USAP

- X A check in the total amount of \$ 690.00 is enclosed to cover filing fee, Recordation of Assignment fee.
- X The Commissioner is hereby authorized to charge to my Deposit Account No. 19-2816 any fees required under any of 37 CFR §§1.16 to 1.17 at any time during the pendency of this application.

Ronald R. Snider Reg. No. 19,

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RRS/gah

ELECTRONIC ENDOSCOPE SYSTEM
ALLOWING ACCURATE DELAY TIME TO BE SET

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an electronic endoscope system, particularly to a configuration for canceling a shift of processing timing of a video signal transmitted from an imaging device at the time of using electronic endoscopes different in length by connecting them.

Description of the Prior Art

An electronic endoscope system is configured by connecting various electronic endoscopes different in observation object to a processor unit for executing image processing. Because these electronic scopes are different in length (including cable length), the processor unit provides a delay time corresponding to the length of an electronic scope for a processing signal in order to adjust processing timing correspondingly to a transmission time of a video signal. Japanese Patent Application of Laid-Open Publication No. 03118023A discloses a conventional system for setting and controlling the delay time.

1 The system of this patent detects scope discriminating
2 information and provides a delay time corresponding to a length
3 of a previously-known electronic scope through tap selection
4 of multitap delay in accordance with the information. In case
5 of a custom electronic scope, a manual adjustment mechanism
6 using a variable resistance is used so as to manually change
7 delay times. As a result, it is possible to correspond to most
8 electronic endoscopes different in length.

9

10 BRIEF SUMMARY OF THE INVENTION

11 Object of the Invention

12 However, a multitap delay circuit used for the above
13 conventional electronic endoscope system has problems that it
14 can only correspond to a preset delay time, delay times which
15 can be set are rough, and an accurate delay time cannot be set.

16 Moreover, setting an adjustment circuit using a variable
17 resistance together with a multitap delay circuit requires
18 adjustment and handling becomes complex because the adjustment
19 must be performed every connection between a conventional scope
20 and a new scope.

21

22 Summary of the Invention

23 The present invention is made to solve the above problems
24 and its object is to provide an electronic endoscope system

1 making it possible to set an accurate delay time corresponding
2 to a length of an electronic scope and moreover simplify the
3 configuration.

4 To attain the above object, the present invention comprises
5 an electronic endoscope to whose front end an imaging device
6 is set, a processor unit connected with the electronic endoscope
7 to apply a predetermined signal processing to a video signal
8 output from the imaging device, a reference-delay-time
9 generation circuit for generating a signal having a rough
10 reference delay time, a short-delay-time generation circuit
11 for generating a signal having a delay time shorter than a
12 reference delay time of the reference-delay-time generation
13 circuit, and a control circuit for generating a delay signal
14 corresponding to the length of the electronic endoscope in
15 cooperation with the delay-time generation circuit and
16 controlling image processing in accordance with the delay
17 signal.

18 The above short-delay-time generation circuit has a
19 plurality of gate delay devices and makes it possible to set
20 a short delay time in accordance with a delay of a signal passing
21 through the gate delay devices.

22 According to the above configuration, by supplying
23 delay-time control data obtained from the electronic endoscope
24 to the reference-delay-time generation circuit and the

1 short-delay-time generation circuit, two delay times generated
2 by the delay-time generation circuits are designated and
3 selected and a value obtained by two delay times is set as a
4 delay time. It is possible to set an accurate delay time by
5 a simple configuration in accordance with the combination and
6 cooperation of these two generation circuits.

7 The above control circuit has a first multiplexer for
8 selecting any one of a plurality of drive clock signals
9 respectively having a reference delay time and a second
10 multiplexer for selecting any one of a plurality of drive clock
11 signals respectively having a short delay time and makes it
12 possible to obtain a delay signal corresponding to the length
13 of the above electronic endoscope by controlling these
14 multiplexers.

15

16 BRIEF DESCRIPTION OF THE DRAWINGS

17 FIG. 1 is a block diagram showing a configuration of an
18 electronic endoscope system of an embodiment of the present
19 invention;

20 FIG. 2 is a circuit diagram showing a configuration of
21 a multiplexer of an embodiment;

22 FIG. 3 is a circuit diagram showing a configuration of
23 a short-delay-time generation circuit and a multiplexer of an
24 embodiment; and

1 FIG. 4 is a signal waveform diagram showing operations
2 of an embodiment.

3

4 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

5 FIGS. 1 to 3 show a configuration of an electronic endoscope
6 system of an embodiment. As shown in FIG. 1, an electronic
7 endoscope (electronic scope) 10 is configured by connecting
8 with a processor unit (this unit may include a light-source
9 unit) 12. A CCD (Charge Coupled Device) 14 is set to the front
10 end of the electronic scope 10 and a CCD drive circuit 15 is
11 provided to read a video signal from the CCD 14.

12 Moreover, the electronic scope 10 is provided with a ROM
13 (Read Only Memory such as EEPROM) 16 for storing various pieces
14 of information by being connected with the processor unit 12
15 to read a video signal and process an image and control data
16 having a delay time corresponding to the length of the electronic
17 scope 10 is stored in the ROM 16. This embodiment stores bit
18 data for directly designating a delay time of each of delay-time
19 generation circuits (24 and 26) to be mentioned later.

20 The processor unit 12 is provided with a microcomputer
21 18 for reading data from the ROM 16 and generally controlling
22 circuits in the unit and moreover provided with a timing-signal
23 generation section 20 for generating a timing signal (drive
24 clock signal) to be supplied to the CCD drive circuit 15 and

1 a timing signal (drive clock signal) having a predetermined
2 delay time and a signal processing circuit 21 for
3 image-processing a video signal input from the CCD 14.

4 The timing-signal generation section 20 includes a timing
5 generator (TG) 23 for generating a base clock signal and a drive
6 clock signal, a reference-delay-time generation circuit 24 for
7 generating a drive clock signal to which a rough delay time
8 is supplied from the base clock signal and drive clock signal,
9 and a multiplexer 25 for selecting a signal obtained by the
10 generation circuit 24 in accordance with the control data sent
11 from the microcomputer 18.

12 FIG. 2 shows an internal configuration of the multiplexer
13 25 which is configured of a logic-arithmetic circuit for
14 selecting a delay time with two-bit control data (the number
15 of bits increases in accordance with the number of selections)
16 25f, AND circuits 25a, 25d, 25b, and 25c, and an OR circuit
17 25g. That is, when it is assumed that four drive clock signals
18 S_A , S_D , S_B , and S_C respectively having a rough delay time are
19 generated by the reference-delay-time generation circuit 24
20 and control data D_1 for which a two-bit delay time is supplied
21 to the logic-arithmetic circuit 25f from the microcomputer 18,
22 any one of outputs Q_1 , Q_2 , Q_3 , and Q_4 becomes High in accordance
23 with the data D_1 . For example, when the output Q_1 becomes High,
24 the reference-delay-time signal (drive clock signal) S_A is

1 output through the AND circuit 25a and OR circuit 25g. When
2 the output Q_2 becomes High, the reference-delay-time signal
3 S_D is output through the AND circuit 25d and OR circuit 25g.

4 Moreover, a short-delay-time generation circuit 26 and
5 a multiplexer 27 are set to the rear stage of the multiplexer
6 25 shown in FIG. 1 and details of these circuits are shown in
7 FIG. 3. In FIG. 3, six gate delay devices 26a, 26b, 26c, 26d,
8 26e, and 26f comprising a CMOS transistor or the like are provided
9 for the short-delay-time generation circuit 26 and outputs of
10 the gate delay device 26a to 26f are connected to input ports
11 1 to 6 of the multiplexer 27.

12 The gate delay devices 26a to 26f delay a signal by a time
13 (minimum time is nano-order) for the signal to pass through
14 a transistor device and thereby, set a delay time shorter than
15 the reference delay time, and output six drive clock signals
16 different in delay time in this case. The number of gate delay
17 devices 26a to 26f is optionally set in accordance with the
18 relation between a delay time of a transistor device used and
19 the reference delay time. In the case of this embodiment, fewer
20 gate delay devices are set in order to simplify description.

21 Moreover, an internal configuration of the multiplexer
22 27 is basically the same as that in FIG. 2, in which three-bit
23 delay-time control data (the number of bits increases in
24 accordance with the number of selections) D_2 supplied from the

1 microcomputer 18 is input from ports H_1 , H_2 , and H_3 to select
2 six drive clock signals whose short delay times are given from
3 the control data D_2 .

4 This embodiment has the above configuration and its
5 functions will be described by referring to FIGS. 4A to 4L.
6 FIGS. 4A and 4B show a base clock and a drive clock output from
7 the timing generator 23 in FIG. 1. A cycle of the drive clock
8 of this embodiment is set to a value two times ($2t_B$) larger
9 than the cycle t_B of the base clock. The reference-delay-time
10 generation circuit 24 generates drive clock signals S_A , S_D ,
11 S_B , and S_C having reference delay times shifted from each other
12 every $1/2 (t_B/2)$ the base clock cycle t_B through logical operation
13 as shown in FIGS. 4C to 4F.

14 In the short-delay-time generation circuit 26, six drive
15 clock signals having a shift of a short delay time t_s passing
16 through one device are generated by the gate delay devices 26a
17 to 26f. For example, when selecting the signal S_C in FIG. 4F
18 obtained by the reference-delay-time generation circuit 24,
19 drive clock signals S_{C1} , S_{C2} , S_{C3} , S_{C4} , S_{C5} , and S_{C6} shifted by
20 a short delay time t_s are generated by selecting the input ports
21 1 to 6 of the multiplexer 27 in FIG. 3 as shown in FIGS. 4G
22 to 4L. Moreover, six signals are similarly generated for other
23 reference-delay-time signals S_A , S_B , and S_D .

1 When the electronic scope 10 is connected to the processor
2 unit 12 having the timing-signal generation circuit 20, any
3 one of the reference-delay-time signals S_A , S_B , S_C , and S_D is
4 obtained when the microcomputer 18 obtains control data
5 (directly designated data) D_1 and D_2 for delay times from the
6 ROM 16 and supplies two-bit control data D_1 to the
7 reference-delay-time generation circuit 24. Moreover, by
8 supplying three-bit control data D_2 to the short-delay-time
9 generation circuit 26, a delay signal more accurately set than
10 the reference delay time is obtained. For example, when the
11 control data D_1 for selecting the signal S_C and the control
12 data D_2 for selecting the input port 3 (multiplexer 27) are
13 input, the drive clock signal in FIG. 4I is output as a delay
14 signal.

15 At the time of selecting the port 0 of the multiplexer
16 27 in FIG. 3, any one of the reference-delay-time signals S_A ,
17 S_B , S_C , and S_D is output as a delay signal. Moreover, the delay
18 drive clock signal is supplied to the signal processing circuit
19 21 and thereby, image processing considering the length of each
20 electronic scope 10 is preferably executed. Thus, this
21 embodiment has an advantage that a delay time can be accurately
22 set by a simple configuration by combining a circuit for
23 generating a rough delay time with a circuit for generating
24 a short delay time.

1 Moreover, this embodiment is configured so as to directly
2 read designated data for a scope delay time stored in the ROM
3 16 of the electronic scope 10. However, when only scope ID
4 data is written, it is also permitted that the microcomputer
5 18 judges a delay time in accordance with ID data so as to generate
6 a predetermined delay-time signal.

7 Furthermore, by reversing positions of the
8 reference-delay-time generation circuit 24 and
9 short-delay-time generation circuit 26, it is possible to
10 generate a delay signal similarly to the above case.

11 According to the above configuration, it is possible to
12 set an accurate delay time corresponding to a length of an
13 electronic scope by a simple configuration.

14

1 What is claimed is:

2 1. An electronic endoscope system comprising:

3 an electronic endoscope to whose front end an imaging device
4 is set;

5 a processor unit connected with the electronic endoscope
6 to apply a predetermined signal processing to a video signal
7 output from the imaging device;

8 a reference-delay-time generation circuit for generating
9 a signal having a rough reference delay time;

10 a short-delay-time generation circuit for generating a
11 signal having a delay time shorter than a reference delay time
12 of the reference-delay-time generation circuit; and

13 a control circuit for generating a delay signal
14 corresponding to a length of the electronic endoscope in
15 cooperation with these delay-time generation circuits and
16 controlling image processing in accordance with the delay
17 signal.

18

19 2. The electronic endoscope system according to claim 1,
20 wherein

21 the short-delay-time generation circuit is provided with
22 a plurality of gate delay devices to set a short delay time
23 according to a delay of a signal passing through the gate delay
24 devices.

1 3. The electronic endoscope system according to claim 1,
2 wherein

3 the control circuit has a first multiplexer for selecting
4 any one of a plurality of drive clock signals generated by the
5 reference-delay-time generation circuit and respectively
6 having a reference delay time and a second multiplexer for
7 selecting any one of a plurality of drive clock signals
8 respectively generated by the short-delay-time generation
9 circuit and respectively having a short delay time, and
10 a delay time corresponding to the length of the electronic
11 endoscope is obtained by controlling the first and second
12 multiplexers.

13

14 4. The electronic endoscope system according to claim 1,
15 wherein

16 the control circuit is set to a processor unit, reads
17 delay-time data for a connected electronic endoscope from the
18 electronic endoscope, and generates a necessary delay signal
19 in accordance with the delay-time data.

20

1 **ABSTRACT**

2

3 This application provides an electronic endoscope system
4 allowing an accurate delay time corresponding to a length of
5 an electronic scope to be set and allowing a configuration to
6 be simplified. The electronic endoscope system is configured
7 by connecting electronic endoscopes different in length to a
8 processor unit and provided with a reference-delay-time
9 generation circuit for generating a signal having a rough
10 reference delay time and a short-delay-time generation circuit
11 for generating a signal having a delay time shorter than the
12 reference delay time by using a gate delay device or the like.
13 A microcomputer in the processor unit reads
14 delay-time-designation control data D_1 and D_2 from a ROM in
15 an electronic scope, generates a delay drive clock signal by
16 the two delay-time generation circuits in accordance with the
17 control data D_1 and D_2 , and executes preferable image processing
18 in accordance with the delay signal.

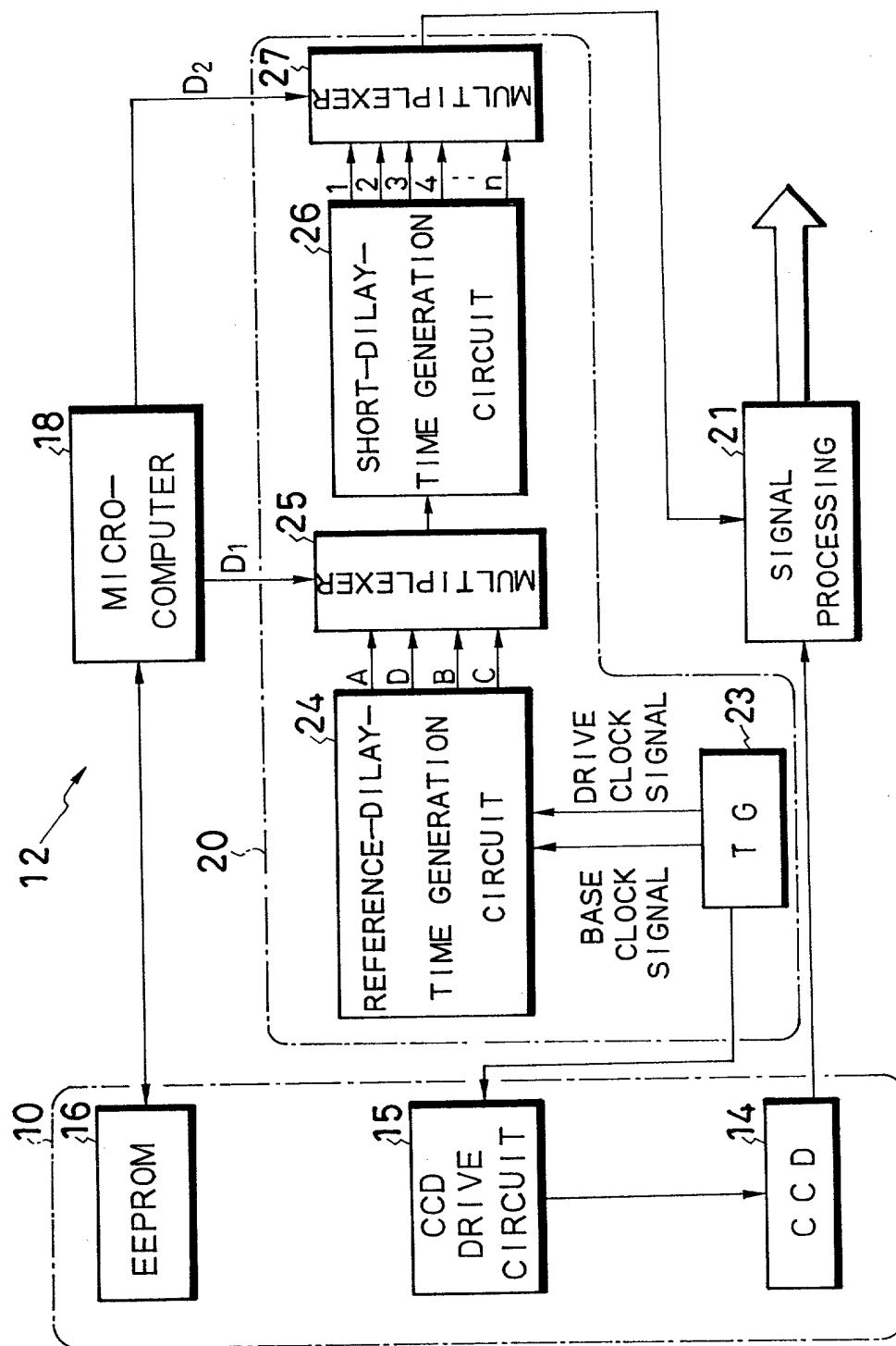
$\frac{1}{4}$ 

FIG. 2

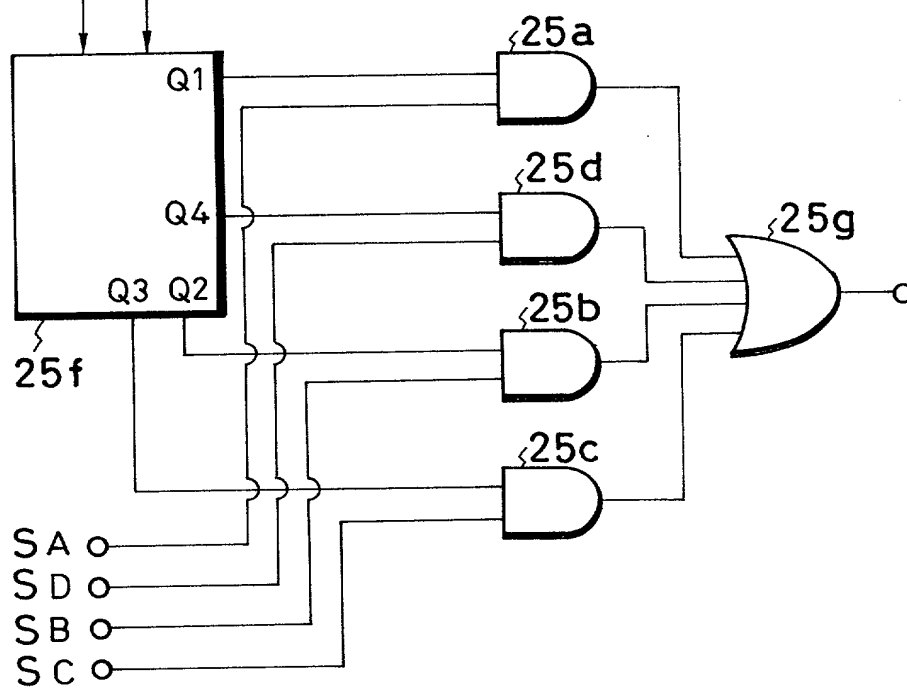
DILAY-TIME-CONTROL
BIT DATA D₁

FIG. 3

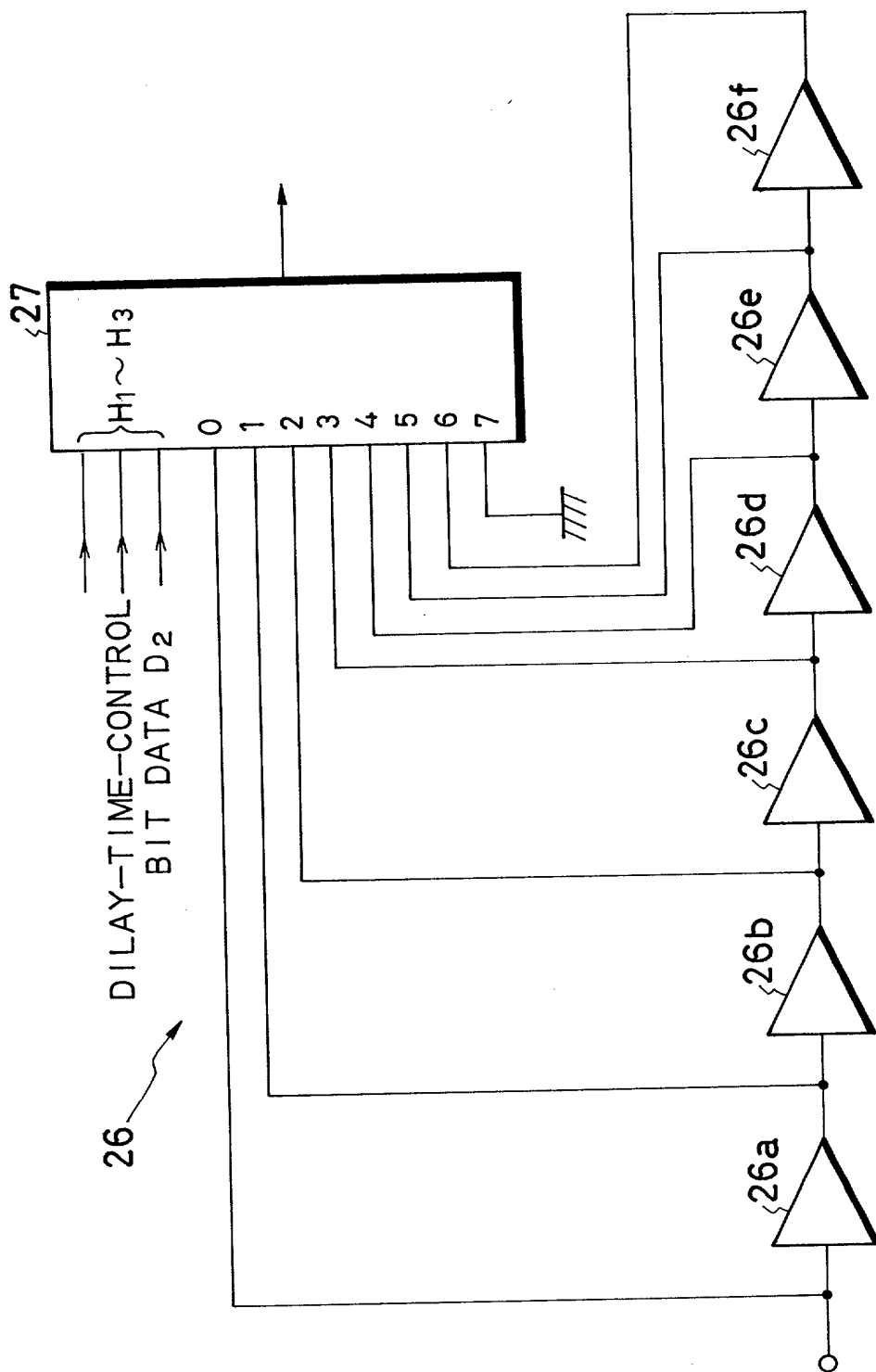
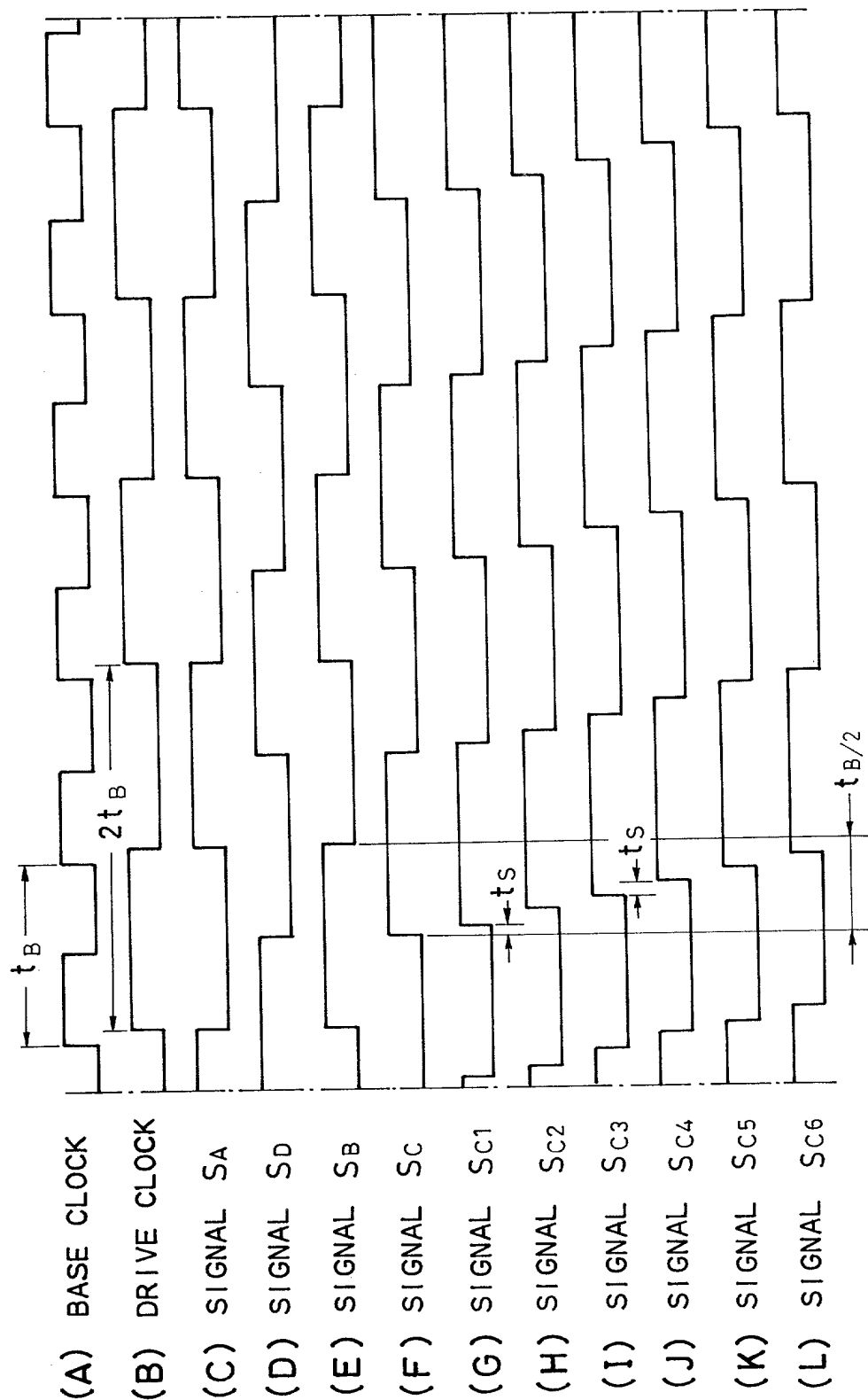


FIG. 4



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PTOSB/01 (8-96)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION

☐ Declaration Submitted with Initial Filing ☐ Declaration Submitted after Initial Filing

Attorney Docket Number

First Named Inventor

Kazunori ABE

COMPLETE IF KNOWN

Application Number

Filing Date

Group Art Unit

Examiner Name

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ELECTRONIC ENDOSCOPE SYSTEM ALLOWING ACCURATE
DELAY TIME TO BE SET

(Title of the invention)

the specification of which

☐ is attached hereto
OR

☐ was filed on (MM/DD/YYYY)

as United States Application Number or PCT International

Application Number

and was amended on (MM/DD/YYYY)

(if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37 Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code § 119 (a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365 (a) of any PCT International application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?	
				YES	NO
11-178440	Japan	6/24/1999	<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	<input checked="" type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>

☐ Additional foreign application numbers are listed on a supplemental priority sheet attached hereto:

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)	<input type="checkbox"/> Additional provisional application numbers are listed on a supplemental priority sheet attached hereto.

(Page 1 of 5)

Burden Hour Statement: This form is estimated to take 0.4 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner of Patents and Trademarks, Washington, DC 20231.

Please type a plus sign (+) inside this box → ☐

DECLARATION

I hereby claim the benefit under Title 35, United States Code § 120 of any United States application(s), or § 385(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application Number	PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number (if applicable)

☐ Additional U.S. or PCT international application numbers are listed on a supplemental priority sheet attached hereto.

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Name	Registration Number	Name	Registration Number
Ronald R. Snider	24,962		
Peter N. Lalos	19,789		
Francis A. Keegan	19,245		

☐ Additional registered practitioner(s) named on a supplemental sheet attached hereto.

Direct all correspondence to:

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Country	United States	Telephone	202-347-2600
		Fax	202-347-7870
		ZIP	20038-7613

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name	Kazunori	Middle Initial		Family Name	ABE	Suffix e.g. Jr.	
Inventor's Signature	<i>Kazunori - ABE</i>					Date	May 29, 2000

Residence: City	Omiya-shi, Saitama	State		Country	Japan	Citizenship	Japanese
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Post Office Address	c/o Fuji Photo Optical Co., Ltd.,
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Post Office Address	1-324, Uetake-machi, Omiya-shi, Saitama, Japan
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City		State		Zip	330-8624	Country	Japan
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☐ Additional Inventors are being named on supplemental sheet(s) attached hereto

Please type a plus sign (+) inside this box → ☐ +

DECLARATION					ADDITIONAL INVENTOR(S) Supplemental Sheet	
Name of Additional Joint Inventor, if any:				<input type="checkbox"/> A petition has been filed for this unsigned inventor		
Given Name	Mitsuru	Middle Initial		Family Name	HIGUCHI	Suffix e.g. Jr.
Inventor's Signature	<i>Mitsuru Higuchi</i>				Date	May 29, 2000
Residence: City	Omiya-shi, Saitama	State		Country	Japan	Citizenship Japanese
Post Office Address	c/o Fuji Photo Optical Co., Ltd.,					
Post Office Address	1-324, Uetake-machi, Omiya-shi, Saitama, Japan					
City		State		Zip	330-8624	Country Japan
Name of Additional Joint Inventor, if any:				<input type="checkbox"/> A petition has been filed for this unsigned inventor		
Given Name		Middle Initial		Family Name		Suffix e.g. Jr.
Inventor's Signature					Date	
Residence: City		State		Country		Citizenship
Post Office Address						
Post Office Address						
City		State		Zip		Country
Name of Additional Joint Inventor, if any:				<input type="checkbox"/> A petition has been filed for this unsigned inventor		
Given Name		Middle Initial		Family Name		Suffix e.g. Jr.
Inventor's Signature					Date	
Residence: City		State		Country		Citizenship
Post Office Address						
Post Office Address						
City		State		Zip		Country
Name of Additional Joint Inventor, if any:				<input type="checkbox"/> A petition has been filed for this unsigned inventor		
Given Name		Middle Initial		Family Name		Suffix e.g. Jr.
Inventor's Signature					Date	
Residence: City		State		Country		Citizenship
Post Office Address						
Post Office Address						
City		State		Zip		Country

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